MARKED-UP COPY OF THE CLAIMS FILED IN THE PRELIMINARY AMENDMENT

1. (Original) A data transmission system comprising:

a mode controller receiving first data having a plurality of bits and outputting a first control signal in accordance with a number of data transitions of the plurality of bits of the data;

a data transmitter coupled to the mode controller and outputting second data corresponding to the first data in response to the first control signal from the mode controller; and

a data receiver coupled to the data transmitter and outputting third data corresponding to the second data in response to a second control signal corresponding to the first control signal.

2. (Original) The data transmission system according to claim 1, wherein the first and second control signals are the same signal.

3. (Original) The data transmission system according to claim 1, wherein the second data is an inverse of the first data depending on the first control signal.

4. (Original) The data transmission system according to claim 1, wherein the third data is an inverse of the second data depending on the second control signal.

5. (Original) The data transmission system according to claim 1, wherein the third data is the same as the first data.

6. (Original) The data transmission system according to claim 1, wherein the mode controller comprises:

transition detecting unit receiving the first data and detecting a transition in the plurality of bits of the first data;

a counter coupled to the transition detecting unit counting the number of transitions in the plurality of bits of the first data;

a comparator coupled to the counter comparing the number of transitions to a reference value; and

an output unit coupled to the comparator and outputting the first control signal.

7. (Original) The data transmission system according to claim 6, wherein the reference value is one of N/2, (N/2-1), and (N/2+1), where N is the number of bits of the first data.

8. (Original) The data transmission system according to claim 6, wherein the transition detecting unit comprises a plurality of transition detecting cells corresponding to the plurality of bits of the first data.

9. (Original) The data transmission system according to claim 8, wherein each of the transition detecting cell includes:

first flip-flop having a first output;

second flip-flop having a second output, the second flip-flop receiving the first output of the first flip-flop; and

a logic unit receiving the first and second outputs from the first and second flip-flops and outputting a third output, the third output containing information on a data transition of a corresponding bit of the plurality of the data bits of the first data.

10. (Original) The data transmission system according to claim 1, wherein the data transmitter comprises a control unit receiving the first data, an inverse of the first data, and the first control signal and outputting the second data, the second data being one of the inverse of the first data or the first data.

11. (Original) The data transmission system according to claim 1, wherein the data transmitter includes a logic unit receiving the first data and the first control signal and outputting the second data, the second data being one of the inverse of the first data or the first data.

12. (Original) The data transmission system according to claim 11, wherein the logic unit includes a plurality of exclusive OR gates.

13. (Original) The data transmission system according to claim 1, wherein the data receiver comprises a control unit receiving the second data, an inverse of the second data, and the second control signal and outputting the third data, the third data being one of the inverse of the second data or the second data.

14. (Original) The data transmission system according to claim 1, wherein the data receiver includes a logic unit receiving the second data and the second control signal and outputting the third data, the third data being one of the inverse of the second data or the second data.

15. (Original) The data transmission system according to claim 14, wherein the logic unit includes a plurality of exclusive OR gates.

16. (Original) A data transmission system for a computer comprising:

a main control unit including:

a video card outputting first data;

a mode controller receiving first data having a plurality of bits and outputting a first control signal in accordance with a number of data transitions of the plurality of bits of the data; and

a data transmitter coupled to the mode controller and outputting second data corresponding to the first data in response to the first control signal from the mode controller; and

a display unit coupled to the main control unit including:

a data receiver coupled to the data transmitter and outputting third data corresponding to the second data in response to a second control signal corresponding to the first control signal; and

data driver coupled to the data receiver and receiving the third data.

17. (Original) A data transmission system for a computer according to claim 16, further comprising an interface unit between the data receiver and the data driver.

18. (Original) A data transmission system for a computer according to claim 16, wherein the data receiver and the data driver are in one unit.

19. (Original) A liquid crystal display device having a data transmission system comprising:

a mode controller receiving first data having a plurality of bits and outputting a first control signal in accordance with a number of data transitions of the plurality of bits of the data;

a data transmitter coupled to the mode controller and outputting second data corresponding to the first data in response to the first control signal from the mode controller; and

a data receiver coupled to the data transmitter and outputting third data corresponding to the second data in response to a second control signal corresponding to the first control signal.

20. (Original) The liquid crystal display device according to claim 19, wherein the first and second control signals are the same signal.

21. (Original) The liquid crystal display device according to claim 19, wherein the second data is an inverse of the first data depending on the first control signal.

22. (Original) The liquid crystal display device according to claim 19, wherein the third data is an inverse of the second data depending on the second control signal.

23. (Original) The liquid crystal display device according to claim 19, wherein the third data is the same as the first data.

24. (Original) The liquid crystal display device according to claim 19, wherein the mode controller comprises:

transition detecting unit receiving the first data and detecting a transition in the plurality of bits of the first data;

a counter coupled to the transition detecting unit counting the number of transitions in the plurality of bits of the first data;

a comparator coupled to the counter comparing the number of transitions to a reference value; and

an output unit coupled to the comparator and outputting the first control signal.

25. (Original) The liquid crystal display device according to claim 24, wherein the reference value is one of N/2, (N/2-1), and (N/2+1), where N is the number of bits of the first data.

26. (Original) The liquid crystal display device according to claim 24, wherein the transition detecting unit comprises a plurality of transition detecting cells corresponding to the plurality of bits of the first data.

27. (Original) The liquid crystal display device according to claim 26, wherein each of the transition detecting cell includes:

first flip-flop having a first output;

second flip-flop having a second output, the second flip-flop receiving the first output of the first flip-flop; and

a logic unit receiving the first and second outputs from the first and second flip-flops and outputting a third output, the third output containing information on a data transition of a corresponding bit of the plurality of the data bits of the first data.

28. (Original) The liquid crystal display device according to claim 19, wherein the data transmitter comprises a control unit receiving the first data, an inverse of the first data, and the first control signal and outputting the second data, the second data being one of the inverse of the first data or the first data.

29. (Original) The liquid crystal display device according to claim 19, wherein the data transmitter includes a logic unit receiving the first data and the first control signal and outputting the second data, the second data being one of the inverse of the first data or the first data.

30. (Original) The liquid crystal display device according to claim 29, wherein the logic unit includes a plurality of exclusive OR gates.

31. (Original) The liquid crystal display device according to claim 19, wherein the data receiver comprises a control unit receiving the second data, an inverse of the second data, and the second control signal and outputting the third data, the third data being one of the inverse of the second data or the second data.

32. (Original) The liquid crystal display device according to claim 19, wherein the data receiver includes a logic unit receiving the second data and the second control signal and outputting the third data, the third data being one of the inverse of the second data or the second data.

33. (Original) The liquid crystal display device according to claim 32, wherein the logic unit includes a plurality of exclusive OR gates.

34. (Original) A computer comprising:

a main control unit including:

a video card outputting first data;

a mode controller receiving first data having a plurality of bits and outputting a first control signal in accordance with a number of data transitions of the plurality of bits of the data; and

a data transmitter coupled to the mode controller and outputting second data corresponding to the first data in response to the first control signal from the mode controller; and

a display unit coupled to the main control unit including:

a data receiver coupled to the data transmitter and outputting third data corresponding to the second data in response to a second control signal corresponding to the first control signal; and

data driver coupled to the data receiver and receiving the third data.

35. (Original) A computer according to claim 34, further comprising an interface unit between the data receiver and the data driver.

36. (Original) A computer according to claim 34, wherein the data receiver and the data driver are in one unit.

37. (Original) A method of transmitting data comprising the steps of:

receiving first data having a plurality of bits and outputting a first control signal in accordance with a number of data transitions of the plurality of bits of the data;

outputting second data corresponding to the first data in response to the first control signal; and

outputting third data corresponding to the second data in response to a second control signal corresponding to the first control signal.

38. (Original) A data transmission apparatus, comprising:

a mode controller for receiving a first data having a plurality of bits and a clock signal to detect a number of transitions of the first data corresponding to the clock signal and for generating a mode control signal having a logic value changing in accordance with the number of transitions;

a data transmitter, responsive to the mode control signal, for selectively inverting the first data and transmitting the inverted data; and

a data receiver, responsive to the mode control signal, for selectively inverting the selectively inverted data from the data transmitter to reconstruct the selectively inverted data into the first data.

39. (Original) A data transmission method comprising the steps of:

receiving a first data having a plurality of bits and a clock signal to detect a number of transitions in the first data corresponding to the clock signal and generating a mode control signal having a logic value changing in accordance with the number of transitions;

selectively inverting the first data in response to the mode control signal and transmitting the inverted data; and

selectively inverting the selectively inverted data in response to the mode control signal and reconstructing the inverted data into the first data.

40. (Original) A liquid crystal display device having a data driver for driving a liquid crystal panel, comprising:

a mode controller for receiving video data having a plurality of bits to detect a number of transitions between a first video data and a second video data and for generating a mode control signal having a logic value changing in accordance with the number of transitions;

a data transmitter, responsive to the mode control signal, for selectively inverting the second video data and transmitting the selectively inverted video data; and

a data receiver, responsive to the mode control signal, for selectively inverting the selectively inverted video data from the data transmitter to reconstruct the inverted video data into the second video data.

41. (Original) A computer system including a liquid crystal display device and a video card for producing video data to be supplied to the liquid crystal display device, said system comprising:

a mode controller for receiving video data having a plurality of bits from the video card to detect a number of bit transitions between a first video data and a second video data and for generating a mode control signal having a logic value changing in accordance with the number of bit transitions;

a data transmitter, responsive to the mode control signal, for selectively inverting the second video data and transmitting the selectively inverted video data; and

a data receiver, responsive to the mode control signal, for selectively inverting the selectively inverted video data inputted, via a transmission line, from the data transmitter and for reconstructing the inverted video data into the second video data.

42. (New) A liquid crystal display device having a data transmission system, comprising:

a mode controller receiving video data having a first set of three video signals of odd data and a second set of three video signals of even data and outputting a control signal in accordance with a number of data transitions of the video data;

a data transmitter coupled to the mode controller, selectively inverting video data in response to the control signal from the mode controller and outputting selectively inverted data;

a data receiver coupled to the data transmitter and outputting reconstructed data corresponding to the selectively inverted data and the control signal; and

a data driver converting the reconstructed data into an analog signal and outputting the analog signal to a liquid crystal panel.

43. (New) The liquid crystal display device according to claim 42, wherein the data receiver and the data driver are integrated as one unit.

44. (New) The liquid crystal display device according to claim 42, wherein the video data is selectively inverted by the data transmitter when the number of data transitions of the video data is greater than a predetermined threshold.

45. (New) The liquid crystal display device according to claim 42, wherein the reconstructed data is inverted when the number of data transitions is greater than a predetermined threshold.

46. (New) The liquid crystal display device according to claim 42, wherein the video data is selectively inverted by the data transmitter when the number of data transitions of the video data is greater than a predetermined threshold, and the reconstructed data is inverted when the number of data transitions is greater than a predetermined threshold

47. (New) A liquid crystal display device having a data transmission system comprising:

a mode controller receiving video data having a plurality of bits and outputting a control signal in accordance with a number of data transitions of the plurality of bits of the video data;

a data transmitter coupled to the mode controller and outputting first data corresponding to the video data and the control signal from the mode controller; and

a data driving circuit having a data driver and a data receiver coupled to the data transmitter, the data receiver selectively inverting the first data in response to the control signal, and the data driver converting the selectively inverted first data into an analog signal and outputting the analog signal to a liquid crystal panel,

wherein the data driving circuit is integrated in one unit and electrically connected to the data transmitter with a flexible printed circuit film.

48. (New) The liquid crystal display device according to claim 47, wherein the video data includes a first set of three video signals of odd data and a second set of three video signals of even data.

49. (New) The liquid crystal display device according to claim 47, wherein the video data is inverted by the data transmitter when the number of data transitions of the plurality of bits of video data is greater than a predetermined threshold.

50. (New) The liquid crystal display device according to claim 47, wherein the first data is inverted when the number of transitions is greater than a predetermined threshold.

51. (New) The liquid crystal display device according to claim 47, wherein the video data is inverted by the data transmitter when the number of data transitions of the plurality of bits of video data is greater than a predetermined threshold, and the first data is inverted when the number of transitions is greater than a predetermined threshold.

52. (New) A method of transmitting data comprising:

receiving video data having a first set of three video signals of odd data and a second set of three video signals of even data;

outputting a control signal in response to a number of data transitions of the video data;

selectively inverting the video data in response to the control signal;

outputting selectively inverted data;

outputting reconstructed data corresponding to the selectively inverted data and the control signal;

converting the reconstructed data to an analog signal; and

outputting the analog signal to a liquid crystal panel.

53. (New) A method of driving a liquid crystal display device comprising:

receiving video data having a first set of three video signals of odd data and a second set of three video signals of even data and outputting a control signal in accordance with a number of data transitions of the video data;

selectively inverting video data in response to the control signal and outputting selectively inverted data;

outputting reconstructed data corresponding to the selectively inverted data and the control signal; and

converting the reconstructed data into an analog signal and outputting the analog signal.

54. (New) The method according to claim 53, wherein selectively inverting video data and outputting reconstructed data are performed by a single integrated unit.

55. (New) The method according to claim 53, wherein the video data is selectively inverted when the number of data transitions of the video data is greater than a predetermined threshold.

56. (New) The method according to claim 53, wherein the reconstructed data is inverted when the number of data transitions is greater than a predetermined threshold.

57. (New) The method according to claim 53, wherein the video data is selectively inverted when the number of data transitions of the video data is greater than a predetermined threshold, and the reconstructed data is inverted when the number of data transitions is greater than a predetermined threshold

58. (New) A method of driving a liquid crystal display device having a liquid crystal panel comprising:

receiving video data having a plurality of bits and outputting a control signal in accordance with a number of data transitions of the plurality of bits of the video data;

outputting first data corresponding to the video data and the control signal from the mode controller; and

selectively inverting the first data in response to the control signal, and converting the selectively inverted first data into an analog signal and outputting the analog signal to the liquid crystal panel,

wherein selectively inverting the first data and converting the selectively inverted first data are performed in a singly integrated unit, and

wherein selectively inverting the first data includes receiving the first data through a flexible printed circuit film.

59. (New) The method according to claim 58, wherein the video data includes a first set of three video signals of odd data and a second set of three video signals of even data.

60. (New) The method according to claim 58, wherein the video data is inverted when the number of data transitions of the plurality of bits of video data is greater than a predetermined threshold.

61. (New) The method according to claim 58, wherein the first data is inverted when the number of transitions is greater than a predetermined threshold.

62. (New) The method according to claim 58, wherein the video data is inverted when the number of data transitions of the plurality of bits of video data is greater than a predetermined threshold, and the first data is inverted when the number of transitions is greater than a predetermined threshold.

REMARKS

The Examiner is thanked for the thorough review and consideration of the pending application. The Office Action dated December 8, 2006 has been received and its contents carefully reviewed. Claims 1-62 are pending. Reexamination and reconsideration of the instant application are respectfully requested.

In items 2 and 3 of the Office Action, claims 42-62 are rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claims 1-41 of U.S. Patent No. 6,335,718. Applicants respectfully traverse this rejection. U.S. Patent No. 6,335,718 is the same patent on which this reissue application is based. Accordingly, U.S. Patent No. 6,335,718 cannot be properly applied against claims 42-62. During a telephone conversation with Examiner Shankar on January 16, 2007, Applicants' representative pointed out that the present reissue application was based on U.S. Patent No. 6,335,718. To overcome this obviousness-type double patenting rejection, Examiner Shankar stated that Applicants should set forth that the patent applied in the rejection is the same patent on which the reissue application is based. Accordingly, Applicants respectfully request withdrawal of the rejection of claims 42-62.

In item 4 of the Office Action, the Examiner states that the reissue oath/declaration filed with this application is defective because it fails to identify at least one error which is relied upon to support the reissue application. Applicants herein submit a supplemental declaration/oath that includes identification of at least one error which is relied upon to support the reissue application. Accordingly, Applicants respectfully submit that the supplemental oath/declaration is in full accordance with 37 C.F.R. § 1.175(a)(1) and M.P.E.P. § 1414.

Also in item 4 of the Office Action, the Examiner states that there is an error in the original oath/declaration in item #4. The oath/declaration states new claims 42-52, however,

there are 62 claims. Applicants herein submit a supplemental declaration/oath that identifies the 62 claims in item #4. Also, the Examiner states that all new claims 42-62 must be underlined in their entirety. Applicants herein submit a copy of marked up claims submitted in the Preliminary Amendment filed December 30, 2003. In this response, the Previously Presented added claims are underlined. Accordingly, Applicants respectfully submit the claims are in full accordance with 37 C.F.R. § 1.173(b)(2).

In item 6 of the Office Action, claims 1-62 are rejected as being based upon a defective reissue Declaration under 35 U.S.C. § 251. The Examiner states the nature of the defects have been previously set forth in the Office Action. As stated above, Applicants herein submit a supplemental oath/declaration that includes the additional information required by the Examiner. Accordingly, Applicants respectfully request withdrawal of the rejection of claims 1-62.

Applicants note the Examiner's statement in item 7 that the original patent, or a statement as to loss or inaccessibility of the original patent, must be received before the reissue application can be allowed. Applicants have filed an offer to surrender the original patent for a reissue application in accordance with 37 C.F.R. § 1.178 on December 30, 2003.

In item 8, the Examiner states a supplemental reissue declaration/oath under 37 C.F.R. § 1.175(b)(1) must be received before the application can be allowed and that receipt of such supplemental reissue declaration/oath will overcome the rejection under 35 U.S.C. § 251. Applicants herein submit a supplemental reissue declaration/oath in full accordance with 37 C.F.R. § 1.175(b)(1) including the acceptable language set forth in item 8.

Finally, Applicants' supplemental oath/declaration includes the claim for foreign priority in item #5. Accordingly, Applicants respectfully submit that the supplemental oath/declaration is in full accordance with 37 C.F.R. § 1.63(c)(2) and M.P.E.P. § 1417.

Applicants believe the foregoing remarks place the application in condition for allowance and early, favorable action is respectfully solicited.

If for any reason the Examiner finds the application other than in condition for allowance, the Examiner is requested to call the undersigned attorney at (202) 496-7500 to discuss the steps necessary for placing the application in condition for allowance. All correspondence should continue to be sent to the below-listed address.

If these papers are not considered timely filed by the Patent and Trademark Office, then a petition is hereby made under 37 C.F.R. §1.136, and any additional fees required under 37 C.F.R. §1.136 for any necessary extension of time, or any other fees required to complete the filing of this response, may be charged to Deposit Account No. 50-0911. Please credit any overpayment to deposit Account No. 50-0911. A duplicate copy of this sheet is enclosed.

Dated: March 8, 2007

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